

24th International Symposium on VLSI Design and Test (VDAT 2020)



Bhubaneswar, India, July 2-4, 2020

Call for Papers

Theme: Chip to System for Edge Computing

VDAT began as a small workshop in the year 1998. In 2005, it acquired the status of a Symposium. The purpose of the Symposium is to promote the advancement of all aspects of VLSI. The 24th International Symposium on VLSI Design and Test (VDAT-2020) will be hosted at IIT Bhubaneswar. The aim of this symposium is to bring academics, researchers, startups, and industrial practitioners together to exchange their ideas in the area of VLSI design, test, and system design. We invite prospective authors to submit their original research papers and reviews of emerging technologies, in standard IEEE double-column format, concerning any branch of VLSI Circuits and Systems which covers a wide range of topics including, but not limited to:

Low-Power Integrated Circuits and Devices

Analog/Digital/Mixed Signal Circuits Low-Voltage Low-Power Sensors and Interfaces Circuit design for reliability Device Modeling and Simulation MEMS/NEMS/MOEMS Devices, Organic Devices

Memory and Computing Processor Design

Memory Design STT-RAM, PC-RAM, R-RAM, and Memristors **Emerging Memory Technologies Neuromorphic Computing** Quantum Computing

VLSI Architectures and System Integration

VLSI Signal Processing Architectures Biomedical and Bio-Inspired Systems RF Integrated Systems Optoelectronic-Circuits and Systems Power Electronics and Systems Control aspects of VLSI Systems Machine Learning Architectures Low-Power IoT Architectures and Systems Compressive Sensing, Wireless Systems

VLSI Testing and Security

Hardware Security and VLSI Design Optimization Hardware Attacks, Detection, Threat Modelling Fault diagnosis and Fault Models DFT and BIST for digital designs Hardware-Based Security Primitive Design Trusted Design Automation, Tools & Information Flow IP Design, quality, interoperability and reuse

FPGA based Design and Embedded Systems

High-Speed Interconnects in Microelectronic Systems Adaptive Computing Using Reconfigurable Fabrics Large-Scale Systems and Power Networks Hardware-Software Co-design Reconfigurable and FPGA Design

System-Level Design

Systems-on-Chip (SoC) Mixed-Mode System-on-Chip Lab-on-Chip, Network-on-Chip Wireless Transceivers. Multimedia Processors Heterogeneous and Homogeneous MPSoCs

Emerging Integrated Circuits and Systems

Artificial Intelligence Accelerators Internet of Things Cognitive Computing Systems Embedded Hardware Security and Cryptography Printed & Flexible Electronics Low Power Nanoelectronics Low Power Edge Computing Systems Wearable and Implantable Circuits Advanced 3D ICs & 3D Packaging

CAD for VLSI

Design Automation and CAD tools Design flows for MPSoCs ML/AI based design-flows and EDA Design automation for DFX Virtual Prototyping CAD of FPGAs High-Level Synthesis

https://conference.iitbbs.ac.in/VDAT2020/



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Advisory Committee

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A David Selvakumar, Senior Director, CDAC Bangalore

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Takeaway

Tutorial: Tutorials are invited on the cutting edge research and technology in the area of advanced materials/devices, circuit and systems. Design Contest: The contest has two divisions. One is to design the analog/digital/RF/mixed signal module using EDA tools and other one is to design and demonstrate the safe and secure intelligent systems using hardware. The forum will provide opportunities to the participants to learn hands on practice for chip to system design (C2SD) and embedded system design using sensors and advanced interface devices. Fellowship (Travel and Registration): The scheme provides an opportunity to applicants to attend the symposium to enhance technical knowledge. The fellowship covers the travel & registration grant. To avail the fellowship, please keep eye on symposium site.

Student Research Forum: Students, including bachelors, masters and PhDs may participate in th is forum through presenting their work for better technical inputs to further improve the quality of work. This forum may also provide an opportunity to the students to establish the network with industry players for job perspective. Startup Forum: This forum will provide the opportunities to participants to get aware of the various schemes/initiatives offered by the states and central government in chip fabrication, electronics manufacturing clusters, IoT, ML and AI etc. The forum will also provide a platform to the participants to explore the funding opportunities from venture capitalist, by presenting their ideas. Women in Engineering Forum: The forum will provide the opportunities to the female participants to accelerate their engagement in the area of chip design and autonomous embedded systems.

Important Dates & Submission Instructions

Regular Papers

Full Paper Submission: March 15, 2020 April 10, 2020 May 15, 2020 Notification of Acceptance: May 1, 2020 Camera Ready Paper: May 10, 2020 May 31, 2020

Tutorial Proposal Submission: March 18, 2020 April 15, 2020 Tutorial Announcement: April 15, 2020 May 15, 2020

Student Research

Full Paper Submission: April 2, 2020 Notification of Acceptance: April 25, 2020 May 15, 2020 Camera Ready Paper: April 30, 2020 May 31, 2020

Design Contest

April 31, 2020 Submission of Design: April 20, 2020 Notification of Acceptance: May 15, 2020 May 31, 2020

Authors are invited to submit original, unpublished research manuscripts on the above topics. Submissions must be done through Microsoft CMT system (https://cmt3.research.microsoft.com/VDAT2020). All papers will be reviewed by at least three members of the program committee, with a double-blind review process. Soft copies of papers should be submitted in PDF format as per the IEEE conference style, manuscripts should not exceed six A4 size pages and should be uploaded online. All accepted papers must be presented by one of the authors in order to be included in the proceedings which will be published in IEEE Xplore.

https://cmt3.research.microsoft.com/VDAT2020